

UNITED STATES DISTRICT COURT  
EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION

NETLIST, INC.

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD, et al.

Defendants.

Civil Case No. 2:22-cv-00293-JRG  
(Lead Case)

**JURY TRIAL DEMANDED**

NETLIST, INC.

Plaintiff,

v.

MICRON TECHNOLOGY TEXAS, LLC, et al.

Defendants.

Civil Case No. 2:22-cv-00294-JRG  
(Member Case)

**JURY TRIAL DEMANDED**

**DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF**

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Y.	IPR2022-00615 Patent Owner Response, dated August 10, 2023
Z.	Plaintiff Netlist, Inc.'s Second Supplemental Disclosure of Asserted Claims and Infringement Contentions, dated February 7, 2023
AA.	Declaration of Harold S. Stone, Ph.D., in Support of Micron's Claim Construction Positions

**All emphasis herein is added unless otherwise noted.**

## INTRODUCTION

Netlist’s claims were cobbled together through years of litigation, serial prosecution, and numerous challenges at the Patent Office. This has resulted in patent claims that are not well-supported and have disjointed language requiring the Court’s involvement to construe. The Court should adopt Defendants’ constructions, which are rooted in the claim language and specifications.

### I. DISPUTED CLAIM TERMS

#### A. “rank” (’912, ’417, and ’215 patents, all cls.)

##### 1. The Court should reject Netlist’s untimely arguments.

Defendants object to Netlist’s new construction of “rank,” which raises several previously-undisclosed disputes. As the table below shows, the only substantive dispute in the JCSS regarding “rank” was whether it must have a “fixed” bit-width. Op. Br. 1; Dkt. 94-1 (Netlist’s JCSS exhibit) at 1, 35, 90; Ex. A at 1, 11, 17. Netlist now argues that the memory devices in a rank must also have multiple memory devices, a “predetermined” width, and be capable of a “partial read.” *Id.*

Defendants	Netlist (JCSS)	Netlist (opening brief)
“an independent set of <i>one or more</i> memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module”	“an independent <i>set of</i> DRAM devices on a memory module that act together to read or write the full, <i>fixed</i> bit-width of the memory module in response to command signals, including chip select signals, issued for one read or write transaction”	A “rank” of “DDR memory devices” is “a <i>predetermined group of</i> DDR memory devices on a memory module that <i>can send or receive</i> a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DDR memory devices on the memory module”

Netlist appears to have formulated its new constructions well in advance of its brief, using Dr. Stone’s deposition as a vehicle to generate supposed extrinsic support. *See* Op. Br. 1-3. Yet, Netlist withheld its changed position, prejudicially denying Defendants a fair chance to develop their own record. Accordingly, the Court should find Netlist waived its new, fundamentally

different claim constructions. *Lodsys, LLC v. Brother Int'l Corp.*, 2013 WL 2949959, at \*19-\*20 (E.D. Tex. June 14, 2013) (finding late-disclosed “constructions to have been waived”).

**2. A “rank” can include one or more memory devices.**

**a) The intrinsic evidence compels Defendants’ construction.**

The intrinsic evidence that a “rank” can include a single memory device is overwhelming. First, the ’215 patent expressly describes and claims “*at least one* first memory integrated circuit in [a] first rank and *at least one* second memory integrated circuit in [a] second rank.” Ex. 2, 3:31-35; 37:34-38. This disclosure directly contradicts Netlist’s argument that “rank” excludes single-device ranks and shows that the ordinary meaning of “rank” at the relevant time could have just one memory device. *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1378 (Fed. Cir. 2019) (“Where multiple patents derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.”).<sup>1</sup>

Second, the ’912 patent’s claims further show that a “rank” can have just one memory device. Most asserted claims require a “first number” of memory devices in a “first number” of ranks, thus permitting the same “number” of memory devices as ranks. *E.g.*, Ex. B, 1:28-31. Also, claim 55 specifies that “each rank . . . comprises a plurality of DDR DRAM chip packages. *Id.*, 5:53-57. If “rank” inherently required multiple memory devices, then the phrase “comprises a plurality” would improperly be rendered superfluous. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006).

Third, the specifications repeatedly contemplate memory modules with two memory devices arranged in two ranks—one device per rank. For example, the ’912 patent illustrates a “conventional memory module” with just two “memory devices ‘a’ and ‘b,’”; because the DQ and

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<sup>1</sup> The ’912, ’215, and ’417 patents all claim priority to application no. 11/075,395. Ex. 1 at (63); Ex. 2 at (63); Ex. 3 at (63).

DQS lines of these memory devices are connected to respective common data and strobe lines 112 and 114, these two memory devices are in separate ranks. Ex. 1, 24:13-24, Fig. 6A. Additionally, all three patents describe an embodiment with two memory devices arranged in two ranks, so that when “the command signal is passed through to the selected rank only” it “is sent to only one memory device or the other memory device.” Ex. 1, 8:48-64; Ex. 2, 16:66-17:13; Ex. 3, 19:14-27. Contrary to Netlist’s suggestion, the patents use the plural in reference to Table 1 because there are multiple devices on the *memory module*, not in each rank. *E.g.*, Ex. 1, 7:56-59. Indeed, the PTAB “disagree[d] with [Netlist]’s interpretation,” finding that the passage “indicates an embodiment in which each rank has one memory device.” Ex. C at 12.

Fourth, the specification directly contradicts Netlist’s argument that a “rank” must have multiple memory devices because, according to Netlist, the ’912 patent is supposedly limited to “DDR memory devices having bit-widths of 4, 8, or 16 bits” and “JEDEC standard memory modules at the time of the invention were 64 or 72 bits wide.” Op. Br. 2. The patents explicitly describe *modules* “having widths of . . . **32 bits**, 64 bits, 128 bits, 256 bits, as well as other widths,” and *memory devices* “having bit of 4, 8, 16, **32**, as well as other bit widths” as “compatible” with the invention.” *E.g.*, Ex. 1, 5:56-62, 6:13-19. Importantly, these disclosures include 32-bit wide memory devices used in 32-bit wide memory modules, which confirms that one memory device can have the same bit width as the entire module—*i.e.*, that there can be one device per rank. *Id.*

Fifth, the cited prior art further confirms that a rank can have one or more memory devices. U.S. Patent No. 6,982,892 (“Lee”), like the ’215 patent, defines a “rank” as having one or more memory devices. Ex. D, 2:60-61 (“*At least one* memory device is attached to each sector or rank.”). Lee is intrinsic evidence because the patents cite Lee on their face. *V-Formation, Inc. v. Benetton Grp.*, 401 F.3d 1307, 1311 (Fed. Cir. 2005); Ex. 1 at (56); Ex. 2 at (56); Ex. 3 at (56).

Sixth, the '912 patent reexamination supports Defendants' construction. The examiner did not construe "rank" as a plurality of memory devices, but instead found that Amidi does not disclose "transmitt[ing] a command signal to only one memory device at a time when there is a plurality of memory devices in a rank" because it has multiple memory devices in a rank. Ex. 10, ¶ 54. The Board's decision likewise did not construe "rank"; it found that Amidi's having multiple memory devices per rank precluded it from satisfying claim 16. Ex. 11 at 76. Read correctly, the examiner's reference to situations "*when* there is a plurality of memory devices in a rank" (as in Amidi) shows that other configurations, with only one memory device per rank, are also possible. Ex. 10, ¶ 54; *cf. Phillips*, 415 F.3d at 1314 ("[T]he claim in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' does not inherently mean objects made of steel.").

Lastly, the PTAB has repeatedly construed "rank" in the '912 and '215 patents to encompass "one or more" memory devices, rejecting Netlist's arguments. Ex. C at 9-12; Ex. E at 29-33; Ex. F at 4-6. The prosecution history "consists of the complete record of the proceedings before the PTO," so these holdings are intrinsic evidence. *Phillips*, 415 F.3d at 1317; *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1360-62 (Fed. Cir. 2017). Despite Netlist's argument that these constructions are tentative, they are the best evidence of "how the PTO . . . understood the patent," *Phillips*, 415 F.3d at 1317, and "[t]he public is entitled to rely upon the public record of a patent in determining the scope of [its] claims," *Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1384 (Fed. Cir. 1998). Netlist's construction seeks to put this Court in direct conflict with the PTAB's construction, which is intrinsic evidence.

The intrinsic evidence thus establishes that a "rank" has "one or more" memory devices.

**b) The extrinsic evidence supports Defendants' construction.**

"Given the clarity of the intrinsic evidence, resort to extrinsic evidence is unnecessary," and Netlist's heavy reliance on extrinsic evidence is misplaced. *Seabed Geosolutions (US) Inc. v.*

*Magseis FF LLC*, 8 F.4th 1285, 1290 (Fed. Cir. 2021). Indeed, Netlist’s evidence is particularly “weak extrinsic evidence for the purpose of claim construction” because most of it is entirely untethered to the asserted patents or their priority dates. *iFLY Holdings LLC v. Indoor Skydiving Germany GmbH*, 2016 WL 3745572, at \*3 (E.D. Tex. Mar. 25, 2016).

For example, Netlist cites two Micron websites from **2014** (Ex. 13) and **2019** (Ex. 12), which are unrelated to the proper legal inquiry: how a skilled artisan no later than **2005** would have interpreted the asserted patents in light of their specific disclosures. *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1299 (Fed. Cir. 2003). Similarly, an IPR involving an unrelated patent with a much later priority date (Ex. 14) and an unrelated specification proposal made years later (Exs. 15-16) are no basis to narrow the term “rank” in the asserted patents (and, in any event, those exhibits are fully consistent with Defendants’ construction because a “set” and “collection” can both comprise one memory device). Nor does Dr. Stone’s testimony help Netlist; he testified that “many definitions” exist for “ranks” and that he was not “asked to opine on” which “meaning of rank” should apply to any asserted patent. Ex. 4, 24:2-24, 33:24-34:24.

Tellingly, the only treatise Netlist cites from the time of the asserted patents unequivocally supports Defendants’ construction. Jacob explicitly states that “a rank of memory is a ‘bank’ of **one or more** DRAM devices that operate in lockstep in response to given command.” Ex. 18 at 413. Netlist attempts to create ambiguity over this definition, Op. Br. at 6, but Jacob eliminates any ambiguity on the very next page (which the PTAB did not consider, *see* Ex. 17 at 30-31), stating that ranks can include “**as few as one device per rank.**” Ex. 18 at 414. Accordingly, the only pertinent extrinsic evidence confirms what the intrinsic evidence establishes: a “rank” can have one or more memory devices. *Id.*

**3. Netlist’s “fixed” bit-width requirement is unsupported.**

Netlist identifies no support for its vague requirement that a rank’s bit-width be “fixed.” Op. Br. 8. None of the patents describe a rank’s bit-width as “fixed,” stating only that each rank “generally ha[s] a bit width.” Ex. 1, 2:16-19; Ex. 2, 2:41-43; Ex. 3, 2:47-49. Further this “fixed” requirement does not appear in any extrinsic definition cited by either party. *E.g.*, Ex. 18, 413-14. Netlist cites two JEDEC standards as allegedly specifying “fixed” widths, but neither refers to “fixed” width ranks. Ex. 9 at 5, 12; Ex. 19 at 6. Netlist frets that if the bit-width is not fixed, the number of memory devices in a “rank” could change, but nothing in the plain meaning of “rank” or in the asserted patents precludes such changes. Indeed, patents contemplate “increasing the number of memory devices per rank.” *E.g.*, Ex. 1, 2:24-27. Netlist simply identifies no disclaimer or lexicography that could justify reading a “fixed” requirement into the term “rank.” *Toshiba Corp. v. Imation Corp.*, 681 F.3d 1358, 1369 (Fed. Cir. 2012).

Further, Netlist never explains what it means for a rank’s bit-width to be “fixed,” when it must be “fixed,” or identifies any reason why this requirement is relevant to the parties’ contentions in this case. Netlist’s unsupported construction thus would only confuse, not assist, the jury.

**4. Netlist’s untimely arguments fail on the merits.**

**a) Netlist’s “pre-determined” requirement**

The patent specifications say nothing about the memory devices in a “rank” being “pre-determined” at some unspecified time. *See generally* Exs. 1-3. Netlist’s argument that “each rank of memory devices” must have “dedicated chip-select signal lines” in Table 1 does not support limiting the claims to these “certain embodiments.” *E.g.*, Ex. 1, 7:56-8:17; *see also Jazz Pharms., Inc. v. Amneal Pharms., LLC*, 895 F.3d 1347, 1361-62 (Fed. Cir. 2018). Netlist does not identify any other alleged support for this limitation. Op. Br. 7-8. Further, Netlist’s proposal is unclear

when the memory devices in a “rank” must be determined to be “pre-determined.” *Id.* The Court should thus decline to read this vague requirement into the term “rank.”

**b) Netlist’s “partial read” argument**

The Court should reject Netlist’s argument that “rank” must be construed to support a “partial read” where “a subset of memory devices . . . sends or receives data.” Op. Br. 9. The patents disclose no “partial” read or write capabilities. *See generally* Exs. 1-3. Netlist’s argument rests on its flawed premise that the embodiment at 8:47-54 of the ’912 patent has a multi-device rank, but “each rank has one memory device” in that embodiment. Ex. C at 12; Ex. 1, 8:48-64. Claim 16 of the ’912 patent, which requires transmitting a command signal to only one memory device at a time, does not support Netlist’s construction. As the PTO noted in allowing this claim over Amidi, this claim does not cover a device with multiple devices per rank. Ex. 10, ¶ 54; Ex. 11 at 76. Further, Netlist fails show that extrinsic testimony from an IPR on an unrelated patent with a much later priority date addressing a hypothetical justifies departing from the meaning of “rank” supported by the intrinsic evidence. Op. Br. 9; *see also iFLY*, 2016 WL 3745572, at \*3. Moreover, the only treatise Netlist cites from the time of the asserted patents unequivocally supports Defendants’ construction. Ex. 18 at 413 (Jacobs explicitly stating that “a rank of memory is a ‘bank’ of one or more DRAM devices that *operate in lockstep* in response to given command.”).

Further, Netlist argued in a ’912 patent IPR that a rank’s devices must all “operate in lockstep to respond to a given command,” omitting any “partial” read or write. Ex. G at 34; Ex. Y at 12-14. Netlist thus disclaimed its belated “partial read” arguments. *Aylus*, 856 F.3d at 1361.

**c) Netlist’s construction of “DDR memory devices”**

Netlist’s construction of “DDR memory devices” in the ’912 patent as limited to “JEDEC specifications in effect at the time of the patent” improperly imports a limitation into the claim.

Although the inventors may have intended their invention to be compatible with contemporaneous standards, the '912 patent never disclaims non-compliant memory modules. *See* Ex. 1, 5:56-6:30.

Further, Netlist's construction contradicts its infringement allegations against products that do not implement the "JEDEC specifications in effect at the time of the patent" (such as DDR4, which was not released until nearly a decade later). Ex. Z at 3-6. Netlist cannot have it both ways; "claims are construed the same way for both invalidity and infringement." *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003). If Netlist wishes to preserve its claims' validity by limiting them to "JEDEC specifications in effect at the time of the patent," Op. Br. 3-4, then devices that do not practice those specifications cannot infringe. The Court should reject Netlist's construction of "DDR memory devices," but if it does not, the construction must govern both infringement and invalidity. *Amgen*, 314 F.3d at 1330.

**B. "signal" and "row[/column] address signal" ('912 patent, all cls.)**

**1. Netlist is bound by its previous construction of "signal."**

In Netlist's case asserting the '912 patent against Google, Netlist agreed to Defendants' construction of signal: "a varying electrical impulse that conveys information from one point to another." Ex. H. Netlist then submitted the agreed construction to the PTO in an IDS in connection with '912 patent reexamination, Ex. I (Cite No. 109), making it part of the intrinsic record. *See Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1303-04 (Fed. Cir. 1997).

Netlist's submission of the agreed construction in an IDS constitutes disclaimer. *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365-67 (Fed. Cir. 2014). In *Golden Bridge*, the patentee agreed to a construction in litigation, then submitted that agreed construction in an IDS in a co-pending reexamination. *Id.* at 1364. In a later litigation, the patentee sought to depart from the construction. *Id.* at 1365. The Federal Circuit held the patentee's submission of "its own stipulated construction of a claim term in the context of the particular patent[] being reexamined"

was “a clear and unmistakable assertion by the patentee to the PTO of the meaning and scope of the term.” *Id.* at 1366. Emphasizing that there is “no meaningful difference between limiting claim scope based on an applicant’s stipulations contained in IDS documents and an applicant’s remarks contained in the IDS itself,” and that the patentee “never notified the PTO that it sought a meaning . . . different from its stipulated construction,” the Federal Circuit held the “submission of [the] stipulation to the PTO” was “a clear and unmistakable disclaimer.” *Id.* at 1366-67. Netlist agreed to a construction of “signal” and submitted that construction to the PTO in an IDS without indicating that it sought another meaning. Ex. H; Ex. I. The Court should adopt that construction.

**2. Netlist’s previous construction properly distinguishes a “signal” and “row[/column] address signal” from the structure used to transmit or receive it.**

Netlist’s previously-agreed construction of “signal” originates from a case involving U.S. Patent No. 7,289,386, which is a parent of the ’912 patent with a substantially identical disclosure. Ex. 1 at (63); Ex. J; Ex. K. There, the dispute centered on whether types of signals (e.g., command and control signals) needed to have “pins of a device *dedicated* for that specific information.” Ex. L, 9-13. The Court agreed with Netlist, rejecting any such requirement. Ex. J.

Despite this history, Netlist takes the diametrically opposite position in this case, conflating the recited “signals” with the “line[s]” carrying them and requiring a “dedicated” or “discrete” line for each type of signal. *See* Op. Br. 12-13. This redefinition of “signal” or “row[/column] address signal” is unsupported. Netlist relies on the mere fact that the specification associates lines with certain types of signals in “certain embodiments,” Op. Br. 13 (citing Ex. 1, 6:55-63, 7:39-53, 8:19-43, Table 1), but nothing in these embodiments constitutes lexicography or disavowal or otherwise justifies limiting the claims. *Toshiba*, 681 F.3d at 1369; *Jazz Pharms.*, 895 F.3d at 1361-62.

Instead, the intrinsic evidence establishes that a “signal” is simply an electrical impulse conveying information, and that a “row address signal” and “column address signal” are defined

by the fact that they convey row and column addresses, respectively—not by any “dedicated” line carrying them. The specification states that the memory module’s “edge connections . . . provid[e] *electrical connections* between the computer system and the components of the memory module,” Ex. 1, 6:5-11, and the claims recite “receiving a set of input control signals from the computer system,” *E.g.*, Ex. B, 1:33-35. Further, even if Netlist’s submissions to the PTO were not dispositive as a matter of disclaimer, they are powerful intrinsic evidence that Defendants’ constructions of “signal” and “row[/column] address signal” are correct. *Personalized Medical Commc’ns, LLC v. Apple Inc.*, 952 F.3d 1336, 1340 (Fed. Cir. 2020).

Although the intrinsic evidence is decisive, the extrinsic evidence further establishes that Defendants’ constructions are consistent with the plain and ordinary meanings of “signal” and “row[/column] address signal” in the relevant context. *E.g.*, Ex. M (“signal[: a] variable electrical parameter, such as voltage or current, that is used to convey information through an electronic circuit or system”); Ex. N (explaining how memory devices include arrays of memory locations addressable by row and column addresses); Ex. O (defining “address” as “[t]he number or name that uniquely identifies a register, memory location, or storage device in a computer”).

Indeed, Netlist never actually disputes that Defendants’ constructions reflect the ordinary meanings of these terms in the context of the ’912 patent. And although Netlist seeks to exclude “packetized” signals, it does not explain how its own constructions (“plain and ordinary meaning”) would supposedly exclude “packetized” signals, or how the jury would know whether the claims cover “packetized” signals without claim construction. *See* Op. Br. 12-13; Dkt. 94-1 at 12, 17. Ultimately, Netlist offers no construction that would exclude “packetized” signals and identifies no disclaimer or lexicography that would justify such a construction. *See id.* The Court should therefore apply the construction of “signal” that Netlist already agreed to and submitted to the

PTO, and reject its attempts to import additional limitations into the claims.

**C. “the logic element generates . . . signals in response [to signals (i)-(iv)]” (’912 patent, cls. 1, 15, 28, 39, 77, 80, 82, 86, 88, 90)**

Netlist amended these claims during reexamination to require that the “logic element generates” specified output signals “in response” to four enumerated signals—(i) “at least one row address signal,” (ii) “bank address signals,” (iii) “at least one chip-select signal,” and (iv) “the PLL clock signal.” Ex. P, 48.<sup>2</sup> Netlist conceded that Amidi discloses logic that generates control signals based on *some* of these four inputs (row address and chip-select signals) but argued that Amidi nevertheless does not meet this limitation because it allegedly does not respond to the other enumerated signals. Ex. P, 52. The Board agreed, allowing Netlist’s amended claims only because it “‘construed the logic element limitation in the conjunctive,’ meaning the logic element responds to *all four* enumerated signals.” See Ex. Q, 13 (quoting Ex. R, 9); Ex. S, 13-14, 18-19.

On appeal, Netlist told the Federal Circuit that “[t]he plain and only reasonable reading” of this limitation “is that the logic element responds to *all four* enumerated signals,” arguing that “Netlist *unequivocally disclaimed any broader meaning* during the reexamination.” Ex. Q, 2. Netlist further stated that “Netlist was unambiguous that the logic element *must ‘use* both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal[s],”” *id.* at 28 (alteration in the original), and that “the specification teaches skilled artisans to *use all four* signals to generate the recited output signals,” *id.* at 34. It is difficult to conceive of a more “clear and unmistakable disclaimer” than Netlist’s statements, and enforcing Netlist’s disclaimer is critical to “ensure[] that the claims are not construed one way in order to obtain their allowance and in a different way against accused infringers.” *SpeedTrack, Inc. v.*

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<sup>2</sup> The precise language of this limitation varies slightly between the independent claims, and Defendants’ constructions account for these differences; however, the differences are immaterial to the parties’ dispute: whether all four enumerated signals must be used. See Dkt. 94-2, 56-76.

*Amazon.com*, 998 F.3d 1373, 1381 (Fed. Cir. 2021) (quotation marks omitted).

Netlist never addresses this decisive prosecution history. Op. Br. 14. Netlist points to embodiments of the '912 patent using less than all four signals, *id.*, but it is no surprise that the '912 patent describes embodiments that practice the broad, pre-amendment claims, but not the narrower claims that survived reexamination. *E.g.*, *N. Am. Container, Inc. v. Plastipak Packaging, Inc.*, 415 F.3d 1335, 1346 (Fed. Cir. 2005) (“[T]he fact that the claims do not cover certain embodiments disclosed in the patent is compelled when narrowing amendments are made in order to gain allowance over prior art.”). Thus, Netlist’s arguments do not negate its unmistakable disclaimer that all four enumerated signals must be used to generate the recited output signals.

**D. “A memory module connectable to a computer system, the memory module comprising” ('912 patent, all cls.)**

A preamble “is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.” *Shoes by Firebug LLC v. Stride Rite Children’s Grp.*, 962 F.3d 1362, 1367 (Fed. Cir. 2020). That is the case here. Netlist’s reliance on the Court’s construction of other patents in *Netlist I* is misplaced. The factors that led the Court to find those preambles limiting—that they “provide antecedent basis for ‘memory module’ when later recited” and that “the claims arguably read on other modular computer devices” are not present here, especially because both parties’ constructions of “rank” are limited to memory modules. Ex. 6, 26-27; Section II.A, *supra*. Thus, Netlist has not shown that the body of the '912 patent claims is structurally incomplete.<sup>3</sup>

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<sup>3</sup> In a single footnote, Netlist alleges that '608 patent claim 1’s preamble is also limiting. However, Netlist has not attempted to show the body of that claim is structurally incomplete.

**E. The Buffer Control Terms ('215 patent, cls. 1, 21; '417 patent, cl. 1).**

Each of the independent claims of the '215 and '417 patents recite “logic” or a “circuit” for “providing first control signals to the buffer to enable communication of ... data ... through the buffer” ('215, cls. 1, 21) or for “transfer[ing] ... data signals ... in response to the data buffer control signal” ('417, cl. 1). The claims make clear that this buffer control-based data transfer requires the buffer to selectively electrically couple the common input data line to a first output data line to a first rank of memory while disabling a second output data line to a second rank of memory—what Netlist calls a “fork-in-the-road.” Op. Br. 18. The '215 patent’s claims recite enabling data transfer to one set of memory devices based on one command signal and enabling data transfer to another set of memory devices based on a second data command signal—*i.e.*, a fork-in-the-road. *See* Ex. 2, cl. 1 (“to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer”). The '417 patent similarly requires circuitry to enable transfer of data between the data bus and the memory devices in *one* of the plurality of ranks—*i.e.*, a fork-in-the-road. *See* Ex. 3, cl. 1 (“transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal”).

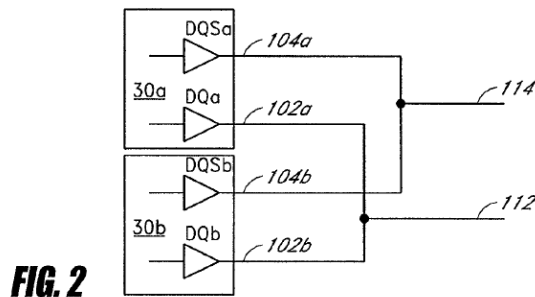
As with the '339 patent in *Netlist I*, the Court should adopt this “fork-in-the-road approach” for the '215 and '417 patents. No. 2:21-CV-00463-JRG, Dkt. 114 at 10. There, the dispute centered on the same issue: “what it means to ‘drive’ [*i.e.*, transfer] data from one side of the buffer to the other.” *Id.* at 9.<sup>4</sup> In adopting the “fork-in-the-road approach” construction, the Court recognized that the '339 patent “[w]hen describing the technological problem to be solved, ...

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<sup>4</sup> Netlist does not dispute that the “buffer” of the '215 patent and the “circuitry” of the '417 patent both constitute a data buffer. *See* Op. Br. 18-20, 24. Netlist asserts no argument against renaming “circuitry” to “data buffer” in Samsung’s construction. *See id.* at 23-24.

emphasizes reducing the load at the outputs of the memory devices.” *Id.* The Court also found “the sole embodiment describing path selection during a write operation disables one path within the buffers when the other path is enabled,” *id.*, and Netlist told the PTO that the “invention ... is about selectively opening otherwise closed data paths,” *id.* at 9. The same is true here.

Like the ’339 patent, the only relevant disclosure in the common specification for the ’215 and ’417 patents is directed to using a buffer to disable a data path for load isolation. Indeed, the section of the specification describing the claimed “buffer” and associated “control signals” is entitled “Load Isolation.” *See* Ex. 3, 5:64; Ex. 2, 5:17.<sup>5</sup> As shown below in Figure 2, the specification depicts “a conventional memory module,” Ex. 2, 6:60-62, where the common data line 112 is always electrically coupled to the memory controller 20 such that “the computer system is exposed to the loads of both memory devices 30a, 30b concurrently.” *Id.* at 7:10-13.

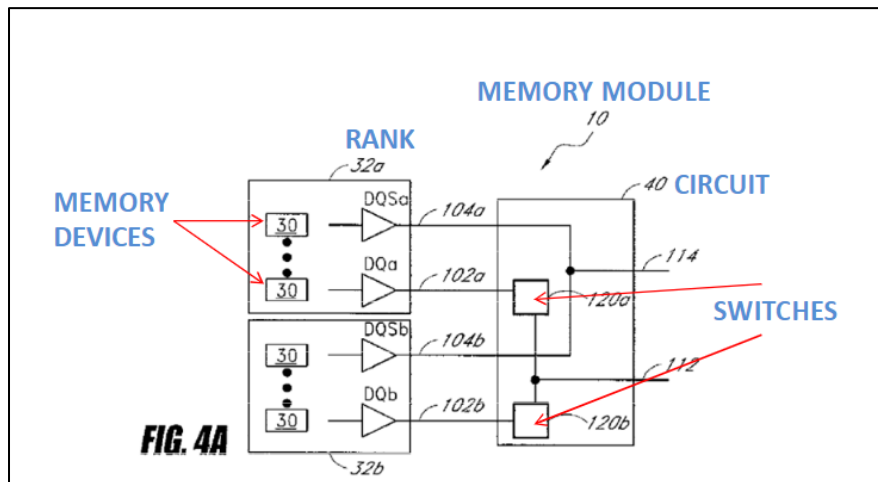


Ex. 2 at Fig. 2; Ex. 3 at Fig. 2. To address this problem, the specification explains, “load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load

<sup>5</sup> The term “control signals” appears only twice in the original specification. Ex. 2, 6:52-55, 8:56-9:3. Netlist added every other instance of “control signal” found in the Abstract and Summary of the Invention of the ’215 patent during prosecution in 2017. *Compare* Ex. T at 68 (original Abstract with no use of “control signals”), *with* Ex. U at 13 (Amended Abstract adding “control signals”); *compare* Ex. T at 13-14 (original Summary with no use of “control signals”), *with* Ex. U at 8-12 (Amended Summary adding “control signals”). As to the ’417 patent, the “control signals” terms in the Abstract and Summary of the Invention first appeared at the time of filing on November 25, 2019. Ex. V at 7-8, 60. Given that Netlist claims priority to 2004, Netlist cannot rely on these new disclosures added over a decade later. *See* 35 U.S.C. §§ 112, ¶2, 120.

... to the computer system *by selectively switching between the two ranks of memory devices 30 to which it is coupled.*” Ex. 3, 10:5-10; Ex. 2, 9:18-23. The specification describes circuit 40 as a “data path rank buffer which advantageously isolates the ranks of memory devices 30 of the memory module 10 from one another.” Ex. 3, 10:15-17; Ex. 2, 9:28-30. In other words, the data buffer uses a fork-in-the-road architecture.

The specification shows that the data buffer uses a fork-in-the-road architecture for enabling load isolation during data transfer. Figure 4A, shown below with Netlist’s own annotations, illustrates this fork-in-the-road architecture. As Netlist told the Federal Circuit, “FIG. 4A below illustrates a memory module with a circuit for selectively electrically coupling a first data signal line to a common data signal line and for selectively electrically coupling a second data signal line to the common data signal line (or, conversely, selectively isolating the loads of memory devices that use the individual data signal lines).” Ex. W at 11.



Ex. W at 12 (Netlist annotations to the same Fig. 4A found in the '215 and '417 patents). Netlist explained that the Fig. 4A switches selectively electrically couple memory devices to the data line:

[U]nlike FIG. 2, the circuit 40 of FIG. 4A includes two switches (120a or 120b) for selectively connecting the device data signal lines (102a, 102b) to the common data signal line (112). Switch 120a can be “selectively actuated to selectively electrically couple” data signal line 102a and common data signal line 112. **When switch 102a is actuated, it electrically connects line 102a and allows electric**

*current to flow to common line 112.... When the switches are not actuated, they isolate the loads of the respective memory devices from the computer system. Thus, each switch allows selective electrical coupling between each respective pair of data lines and selective isolating of the loads of the corresponding memory devices.* Because the memory module's circuit 40 can selectively electrically couple each pair of data lines or selectively isolate the devices' loads, the total electrical load ... that is seen by the computer system can be reduced.

*Id.* at 12-13 (citations omitted).

Consistent with Netlist's characterization, circuit 40 "selectively isolates one or more of the DQ data signal lines 102a, 102b of the two ranks 32a, 32b from the common DQ data signal line 112 coupled to the computer system." Ex. 3, 9:7-9; Ex. 2, 8:27-29; *see also* Ex. 3, 9:13-18; ("[T]he circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first rank 32a or a second DQ data signal from the DQ data signal line 102b of the second rank 32b to be transmitted to the memory controller 20 via the common DQ data signal line 112."); Ex. 2, 8:33-38 (same). And Figures 3A through 5D, 8C, and 8D consistently show the same fork-in-the-road architecture for data signals enabling load isolation.

The specification also consistently discloses that the claimed "control signals" are to enable the fork-in-the-road. The only recitation for "control signals" in the original specification relates to signals that control the switches for electrically coupling/isolating data lines. Ex. 3, 7:32-35 ("[T]he circuit 40 further comprises ... switches ... operatively coupled to the logic element to receive **control signals** from the logic element."); Ex. 2, 6:52-55 (same); Ex. 3, 9:46-50 ("[S]witches 120 are operatively coupled to the logic element 122 to receive **control signals** from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line."); Ex. 2, 8:56-9:3 (same).<sup>6</sup> The buffer control terms should be construed

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<sup>6</sup> Although the disclosure says coupling "one or more" data signal lines to a common data signal line, every use of the control signal in the context of the figures (FIGS. 3A, 3B, 4A, 4B,

consistent with the intrinsic record, which shows the claimed “buffer” and related “[buffer] control signals” transfer data using the fork-in-the-road approach. *See Ruckus Wireless, Inc. v. Innovative Wireless Solutions, LLC*, 824 F.3d 999, 1003-04 (Fed. Cir. 2016) (holding “communications path” could not include wireless communication where all embodiments disclosed wired communications and, construing the claims to include wireless communication “would likely render the claims invalid for lack of written description”); *Eon-Net LP v. Flagstar Bancorp.*, 653 F.3d 1314, 1321 (Fed. Cir. 2011) (limiting “document” and “file” to “information that originates from a hard copy document” where “[t]he written description repeatedly and consistently defines the invention as a system that processes information derived from hard copy documents”).

Netlist’s prosecution statements also demonstrate that the terms are limited to using the fork-in-the-road architecture to enable load isolation. Netlist appealed two final written decisions from the PTAB of two parent patents, U.S. Patent Nos. 7,881,150 and 8,081,536, sharing the same original specification as the ’215 and ’417 patents. Netlist told the Federal Circuit that “[a]dding the configurability to selectively electrically couple a device data line to a common data line was **a key contribution of the inventions.**” Ex. W at 41.<sup>7</sup> Netlist explained “[s]olving the problem of increased loading due to additional memory devices was essential to overcoming the shortcomings

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5A-5D) selects only one output data signal line. There is no disclosure as to how to use the control signal in relation to the switches to select two output data lines or how that would even work. Even the text describing Netlist’s chosen embodiments, Figures 8A and 8B, explain that if more than one rank were selected simultaneously, they would be involved in “collisions or interference.” *See* Ex. 3, 13:60-67, 14:47-55; Ex. 2, 12:5-12, 12:35-43.

<sup>7</sup> “[P]rosecution disclaimer may arise from disavowals made during the prosecution of ancestor patent applications.” *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1333 (Fed. Cir. 2003). Moreover, a patent owner is subject to disclaimer when it surrenders claim scope through argument during post-grant proceedings and appeals therefrom. *See Aylus*, 856 F.3d at 1359-64 (relying on patentee statements in post-grant proceedings to find prosecution disclaimer); *Prism Techs. LLC v. AT & T Mobility, LLC*, 2013 WL 3930002, \*11-\*12 (D. Neb. 2013) (applying patent disclaimer to child patent based on patent owner arguments made to the Federal Circuit on appeal from the PTO).

of prior art memory modules,” and “using hard-wired, permanent data lines [*i.e.*, without a fork-in-the-road to achieve load isolation] is what the specification explains was done in a conventional memory module.” *Id.* at 42, 45. This is the same benefit that Netlist identifies for the ’215 and ’417 patents in this case: “A key technical benefit is ‘load isolation.’” Ex. X at 3.

Netlist should not be permitted to read the invention out of the claims to cover conventional memory modules without a fork-in-the-road. *See Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1315-16 (Fed. Cir. 2007) (holding disclaimer applied to related patent where patentee’s statements “w[ere] not associated with particular language from [the] claims” but instead directed to the “present invention”); *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1368 (Fed. Cir. 2007) (limiting child patent claims to pellet-based implementations where “applicants [in parent applications] repeatedly distinguished the invention from the prior art by referring to the pellet form or ... process as an essential part of the invention”); *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 (Fed. Cir. 1998) (holding that when a patentee distinguishes its “invention” over the prior art rather than distinguishing a specific claim, the disclaimer applies to all claims).

Attempting to counter this powerful intrinsic evidence, Netlist cites the Abstract of the ’215 patent to argue that the claimed “buffer” broadly “enable[s] communication.” Op. Br. 20. Netlist added this language to the Abstract in 2017, Ex. U at Examiner’s Amendment Page 7, and it is not part of the specification on which Netlist relies for priority. Moreover, the claim language requires use of “control signals,” which the specification discloses using only to operate a fork-in-the-road. Netlist also points to Figures 8A and 8B as examples of circuits without load isolation. Op. Br. 20. But these figures are not relevant to the claim terms at issue because they do not use the claimed “[buffer] control signals” for “enabl[ing] communication of” or “transfer[ing]” the claimed “data.” Ex. 3, cl. 1; Ex. 2, cls. 1, 21. Figures 8A and 8B relate to controlling data strobe

(DQS) signals, not data signals (Ex. 3, 15:5-16), and their accompanying text never so much as mentions “control signals.”

For these reasons, the Court should adopt Samsung’s construction.

**F. “Data Buffer Control Signals” (’417 patent, cls. 1, 3, 11)**

The Court should construe “data buffer control signals” consistent with the written description, which solely uses these signals to selectively electrically couple the input data line to one of two output data lines connected to different ranks. The term “data buffer control signals” does not appear in the original specification to which Netlist claims priority. It only appears in the Abstract and the Summary of the Invention added on November 25, 2019. Ex. V at 7-8, 60. The only possible support for this term is found in the original specification’s disclosure of “control signals.” As discussed, the original specification refers to “control signals” only twice and explains that these signals actuate switches to selectively electrically couple or isolate data lines. Ex. 3, 7:32-35; *id.*, 9:46-50. The term “data buffer control signals” must be construed consistently with this limited disclosure. *Ruckus Wireless*, 824 F. 3d at 1004. Any other construction “would likely render the claims invalid for lack of written description.” *Id.* Moreover, Netlist cannot escape its prosecution statements that describe the invention as requiring a fork-in-the-road implementation. *See* Section I.E *supra*.

Netlist has no basis for rejecting Samsung’s construction. Netlist has put forth no evidence that this term has an ordinary meaning in the art that would depart from the patent’s limited disclosure. Instead, Netlist argues that Samsung’s construction would exclude the embodiments of Fig. 8A and 8B. As explained above, Figures 8A and 8B do not use such signals or even control data transfer. Thus, contrary to Netlist’s suggestion, Samsung’s construction does not exclude preferred embodiments that use “data buffer control signals.”

**G. “operable in a computer system to communicate data” (’215 patent, cl. 1; ’417 patent, cl. 1)**

The dispute over “operable ... to” term is whether it requires mere capability (including after modification) or whether it requires structure that presently is configured to perform the recited function. “As to the terms ‘operable’ and ‘operable to,’ ... the applicable principle is: ‘that a device is capable of being modified to operate in an infringing manner is not sufficient, by itself, to support a finding of infringement.’” *TQ Delta, LLC v. CommScope Holding Co., Inc.*, No. 2:21-CV-309-JRG, 2022 WL 2071073, at \*9 (E.D. Tex. June 8, 2022) (quoting *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1330 (Fed. Cir. 2001)). Consistent with this principle, this Court in *TQ Delta* found “‘operable to’ should be construed to refer to being configured to operate in the recited manner.” *Id.* The Court should apply this principle here.

Netlist is wrong that this Court’s holding in *TQ Delta* is inapt. Netlist admits that the concern in that case was whether the construction could be “interpreted broadly as allowing for an ability that arises after modification.” Op. Br. 27-28. Netlist assures the Court that such a “concern is not present here.” *Id.* at 28. If that is true, Netlist should agree to Defendants’ construction, which resolves the same ambiguity. Netlist instead resists Defendants construction by inexplicably labeling it “nebulous.” *Id.* at 27.<sup>8</sup> The Court can and should resolve this ambiguity by adopting Samsung’s proposed construction.

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<sup>8</sup> Moreover, the fact that the word “configured” appears elsewhere in the claims does not give Netlist license to interpret “operable . . . to” inconsistent with Federal Circuit precedent. “The preference for giving meaning to all terms . . . is not an inflexible rule that supersedes all other principles of claim construction.” *SimpleAir, Inc. v. Sony Ericsson Mobile Commc’ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016) (internal citation omitted).

H. “[W]herein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices” (’417 patent, cl. 1) is indefinite.<sup>9</sup>

This term is indefinite under both parties’ proposals for the CAS latency terms. Under Micron’s proposal: **overall** CAS latency relates to the delay between when a read command is executed by the memory module and when the first piece of data is available at an output of the memory module. Similarly, **actual operational** CAS latency relates to the delay between executing a read command by the memory ICs and when the first piece of data is available at an output of the memory ICs. Using these understandings, the disputed claim term at issue is indefinite because a POSITA would not understand the term with reasonable certainty. Specifically, the claim recites read and write commands. It is nonsensical to “register” data to **be written** “for an amount of time delay” such that comparisons of overall to actual CAS latencies (relating to read latencies) are shown to be greater.

A POSITA would similarly not be able to understand the term under Netlist’s “plain and ordinary meaning” proposal. Netlist apparently believes that the plain and ordinary meaning of overall CAS latency means the delay between when a command is sampled on the memory module and when the first piece of data is available at the data pins of the module. *Netlist, Inc. v. Micron Technology, Inc., et al.*, C.A. No. 1:22-cv-134, Joint Claim Construction Statement, Dkt. 65-1, 8-9 (W.D. Tex. Apr. 14, 2022). For a write command, data is “sampled” upon receipt of the data by a memory module – which is the exact same time as “when the first piece of data is available at the data pins of the module.” In other words, there is no time delay for overall CAS latency under Netlist’s interpretation, and registering data being transferred through the circuitry could never make a zero delay greater than **anything**.

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<sup>9</sup> Micron position only.

**I. “overall CAS latency” / “actual operational CAS latency” (’215 patent, cls. 3, 4, 24, 25; ’417 patent, cl. 1)<sup>10</sup>**

The intrinsic record is silent as to the meaning of these terms, and the terms are not well-known terms of art. Ex. AA (Stone Decl.), ¶ 43. Netlist’s plain and ordinary meaning is therefore unhelpful.

Netlist disputes that the terms were understood in reference to read commands, but that is exactly how the terms were understood at the relevant time by the industry. Ex. AA, ¶¶ 44-45. Around the 2004–2005 timeframe, the most relevant standards known to a POSITA were related to Double Data Rate (DDR) and DDR2 memory technology. *Id.* These are the best sources of extrinsic evidence to “help educate the court regarding the field of the invention and [] help the court determine what a [POSITA] would understand claim terms to mean.” *Phillips*, 415 F.3d at 1319. The standards specify that CAS latency was generally synonymous with “Read Latency.” The definition for “Read Latency”/CAS Latency (CL) in the DDR standard is “the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data.” Ex. AA, ¶ 45; Ex. 4 at 10; *see also id.* at 11 (illustrating CAS latency (CL)). Similarly, the standards specify that “[i]n a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency).” Ex. AA, ¶ 45; Ex. 5 at 68. The foregoing clarifies what is meant by the “overall CAS latency”/“actual operational CAS latency” terms and supports Micron’s proposals. Ex. AA, ¶ 45.

Netlist’s citations to disclosures regarding read and write commands is inapposite. *Op. Br.*, 29. That fact is not disputed. Memory devices performed read and write operations at the relevant time. Micron’s construction does not exclude write commands, it instead accurately sets

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<sup>10</sup> Micron position only.

forth a POSITA’s understanding of the claim term as a parameter of a memory system that performs read and write commands. As shown by the extrinsic evidence, CAS latency was only associated with Read Latency around the 2004–2005 timeframe. Netlist’s construction seeks to improperly broaden the CAS latency constructions outside of the known context. Ex. AA, ¶¶ 44-45. Netlist’s reference to Micron’s expert’s testimony regarding CAS latency applying to both read and write data transfers in the specification (Op. Br., 29) is a red herring. While CAS latency was only associated with Read Latency (RL) at the relevant time, Write Latency (WL) was a concept that was defined *in terms of* Read Latency. Netlist admits as much. *Id.* at 30 (citing “Ex. 8 (JESD79-2) at 24 (defining the following relationship:  $WL = RL - 1$ .”).

**J. “burst of data strobe signals” (’215 patent, cls. 12, 13, 28, 29)<sup>11</sup>**

The claims *fail* to inform a POSITA “about the scope of the invention with reasonable certainty.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 908-910 (2014). The parties appear to agree that this term is susceptible to multiple different interpretations—“a set of consecutively transmitted strobe signals originating from (1) two different memory devices with their strobe pins tied together (‘combined strobe’) or (2) a single memory device (‘non-combined strobe’).” Op. Br., 26 (“the claims can properly include both ‘types’ of strobe signals”). But if both distinct “types” of strobe signals could allegedly apply to the term “burst of data strobes,” the claims fail to inform, with reasonable certainty, a POSITA the scope of the invention. Ex. AA, ¶¶ 47-49. The different meanings are material because the entire infringement and invalidity analyses will differ based on which interpretation is ultimately adopted, i.e., each interpretation will require mapping different mutually exclusive configurations of structures and

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<sup>11</sup> Micron position only.

signal lines (e.g., memory devices with their strobe pins tied together (“combined strobe”) vs. memory devices with their strobe pins not tied together (“non-combined strobe”)).

Because the term “burst of data strobes” can take on two materially different meanings, and the claims fail to inform with reasonable certainty which meaning to apply, the claims that use the term are indefinite. *See Dow Chem. Co. v. Nova Chems. Corp. (Can.)*, 803 F.3d 620, 634-35 (Fed. Cir. 2015) (claims indefinite where multiple ways to measure a claimed coefficient and no guidance as to how the coefficient should be measured); *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1343-45 (Fed. Cir. 2015) (claim indefinite where molecular weight could mean three different things that would each yield different results).

**K. “the at least one of the circuit components” (’215 patent, cl. 15)<sup>12</sup>**

The term “the at least one of the circuit components” lacks antecedent basis and is therefore indefinite. *Bushnell Hawthorne, LLC v. Cisco Sys., Inc.*, 813 F. App’x 522, 525-527 (Fed. Cir. 2020). It is unclear whether the claim meant to recite “wherein ~~the~~ at least one of the circuit components is configured to provide” or “~~the at least one of the circuit components is~~ are configured to provide,” or something else entirely. The claim therefore is subject to multiple disparate meanings and should be held indefinite. The specification fails to provide any clarity because it does not disclose any single component of a buffer for providing both first/second data paths in response to first/second control signals.

**L. “logic” (’215 patent, cl. 1; ’417 patent, cl. 1)<sup>13</sup>**

The “logic” limitations are means-plus-function limitations governed by 35 U.S.C. § 112, ¶ 6. The limitations recite a generic term (“logic”) that provides no known structure for performing the associated claimed functionality. Because the ’215 and ’417 patents’

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<sup>12</sup> Micron position only.

<sup>13</sup> Micron position only.

specification fails to describe corresponding structure for the “logic” limitations, claim 1 of the ’215 patent and claim 1 of the ’417 patent are indefinite.

Netlist contends that a POSITA would understand “logic” in general to include a wide range of exemplary structures. Op. Br., 16-17. But that does not negate the fact that the “logic” limitations are claimed in a purely functional manner and fail to recite sufficient structure for performing the claimed functionality. Applying the Federal Circuit’s reasoning in *Williamson*<sup>14</sup> and *Egenera*<sup>15</sup> to the “logic” limitations confirms they are means-plus-function limitations.

The Federal Circuit has recently determined that the specific limitation “logic to . . .” is a means-plus-function limitation under the standard set forth in *Williamson*. *Egenera*, 972 F.3d at 1375. For the same reasons as in *Egenera*, the “logic” limitations here are means-plus-function limitations. For example, as found by the *Egenera* court, the term “logic” does not alone “amount[] to sufficient structure for performing [the claimed] function[s].” *Id.* at 1374 (internal quotations omitted). Instead, the term “logic” as used here, just like the term “logic” at issue in *Egenera* and the term “module” at issue in *Williamson*, “is no more than a ‘black box recitation of structure’ that is simply a generic substitute for ‘means.’” *Id.* at 1375 (quoting *Williamson*, 792 F.3d at 1350). Indeed, as demonstrated by Netlist’s citations to Micron’s expert’s testimony, *see, e.g.*, Op. Br., 17, a POSITA would understand the term “logic” in the “logic” limitations to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the logic limitations. Ex. AA, ¶ 34. Therefore, “logic” does not impart any structure, let alone a sufficiently definite structure, nor a sufficient structure that performs the claimed functions. Instead, “logic” is simply another generic “nonce word[] that reflect[s] nothing more

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<sup>14</sup> *Williamson v. Citrix Online, LLC*, 792 F.3d 1339 (Fed. Cir. 2015).

<sup>15</sup> *Egenera, Inc. v. Cisco Sys.*, 972 F.3d 1367 (Fed. Cir. 2020).

than verbal constructs.” *Williamson*, 792 F.3d at 1350; *see also MTD Prods.*, 933 F.3d at 1343 (claim language reciting what a nonce term is “configured to” do is functional).

The language “coupled to the buffer” and the language “coupled to the printed circuit board” do not impart sufficiently definite structure into the term “logic,” and therefore do not take the overall claim limitations out of the ambit of § 112, ¶ 6. *See Williamson*, 792 F.3d at 1351. For example, in *MTD Products*<sup>16</sup>, the Federal Circuit held, in a much closer case than here, that “[w]hile the claim language reciting that the mechanical control assembly is ‘coupled to the left and right drive units’ connotes structure, the claim language reciting what the mechanical control assembly is ‘configured to’ do is functional.” *MTD Prods.*, 933 F.3d at 1343. The same is true here. That is, the claim language reciting what the “logic” is “configured[/configurable] to” do is purely functional. *See id.* Thus, similar to the finding in *MTD Products*, “the claim format tends to favor [the] position that § 112, ¶ 6 applies.” *Id.*; *see also Williamson*, 792 F.3d at 1351.

The remaining claim language associated with the “logic” fails to describe any structure for performing the claimed functions. Ex. AA, ¶ 35. For example, the claims do not describe how the “logic” interacts with other claimed components to perform the claimed functionality so as to inform a POSITA of the structural character of the “logic.” *Id.* The remaining claim language associated with the “logic” merely recites what the “logic” is configured to do. But this language recites only functionality, i.e., no other structural components.

Similarly, Netlist’s citations to the specification and to general functionality of logic do not take the overall “logic” claim limitations out of the ambit of § 112(6). “The standard is whether the *words of the claim* [not the specification] are understood by [a POSITA] to have a sufficiently definite meaning as the name for structure.” *Williamson*, 792 F.3d at 1349 (emphasis added). In

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<sup>16</sup> *MTD Prod. Inc. v. Iancu*, 933 F.3d 1336 (Fed. Cir. 2019).

any case, the Federal Circuit has already considered the implications of such broad disclosure in a specification and has still held that a “logic” limitation associated with such disclosure is still subject to § 112(6) claim construction. *Egenera*, 972 F.3d at 1374.

Regarding corresponding structure, because § 112, ¶ 6 applies, claim 1 of the ’215 patent and claim 1 of the ’417 patent are indefinite unless their specifications disclose sufficient “corresponding structure” to perform the claimed functions. *Williamson*, 792 F.3d at 1351-52. They do not. Therefore, the claims are indefinite.

A structure qualifies as a “corresponding” structure only if the specification clearly links that structure to the claimed function. *Noah Sys. Inc. v. Intuit Inc.*, 675 F.3d 1302, 1311 (Fed. Cir. 2012). A means-plus-function limitation is indefinite if a POSITA “would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim.” *Id.* at 1312.

Here, the specifications of the ’215 and ’417 patents fail to describe any structure ***corresponding to the claimed functions*** of the means-plus-function “logic” limitations. Ex. AA, ¶¶ 37-42. For example, Netlist’s citations to the specifications of the ’215 and ’417 patents merely identify numerous places where logic is ***generally described*** in the ’215 and ’417 patents’ specification. *See* Op. Br., 18. However, nowhere in the disclosure of the ’215 and ’417 patents cited by Netlist, or anywhere else, is there ***any disclosure of any structure that performs the specific claimed “logic” functionality***, such as, “respond[ing] to the first memory command by ***providing first control signals to the buffer*** to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer.” *Id.* Indeed, Netlist’s string citation falls far short of showing a clear link or association

between a structure in the '215 and '417 patents' specification and the "logic" functionality at issue here. As such, the "logic" limitations are indefinite.

**M. "circuitry" ('417 patent, cls. 1, 6, 11)<sup>17</sup>**

The "circuitry" limitations of claims 1, 6, and 11 are means-plus-function limitations governed by 35 U.S.C. § 112, ¶ 6. The limitations recite a generic term ("circuitry") that provides no known structure for performing certain associated claimed functionality. Because the '417 patent's specification fails to describe corresponding structure for the "circuitry" limitations, claims 1, 6, and 11, and the claims that depend on them, are indefinite.

When a claim term recites a function without reciting sufficient structure for performing that function, the presumption against means-plus-function claiming falls, and means-plus-function claiming applies. *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364 (Fed. Cir. 2013). With respect to the word "circuit," "the pivotal issue is 'whether the [circuit limitation] as properly construed recites sufficiently definite structure.'" *Id.* The "circuitry" limitations at issue here are purely functional and fail to recite sufficient structure for performing the claimed functionality. As such, the limitations invoke § 112, ¶ 6.

Applying the Federal Circuit's reasoning in *Williamson* to the "circuitry" limitations confirms they are means-plus-function limitations. First, Netlist drafted the "circuitry" limitations in a format consistent with traditional means-plus-function limitations. *See MTD Prods.*, 933 F.3d at 1343.

Second, "circuitry" is a generic nonce term that does not alone provide any indication of structure for performing the claimed functions. Although some courts have found the term "circuit" to connote structure when used with an appropriate identifier, there is no hard and fast

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<sup>17</sup> Micron position only.

rule, and the “circuitry” limitations of the ’417 patent are not even prefixed with appropriate identifiers or modifiers. *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364 (Fed. Cir. 2003) (“[W]e do not find it necessary to hold that the term ‘circuit’ by itself always connotes sufficient structure”). At least two courts have found that claim language did not provide sufficient structural support when “circuit” was used, as here, in its generic sense. *See Limestone Memory Sys.*, No. 8:15-CV-00278, 2019 WL 6655273, at \*18–19; *Koninklijke Philips N.V. v. ZOLL Lifecor Corp.*, No. 2:12-CV-1369, 2015 WL 12781199, at \*14 (W.D. Pa. Aug. 28, 2015); Ex. AA, ¶ 52 (“circuitry” is used here in a generic sense, without connoting any specific structure for performing the claimed functions).

The remaining claim language associated with the “circuitry” fails to describe any structure for performing the claimed functions. Ex. AA, ¶ 53. For example, the claims do not describe how the “circuitry” interacts with other claimed components to perform the claimed functionality so as to inform a POSITA of the structural character of the “circuitry.” *Id.* The remaining claim language merely recites what the “circuitry” is configured to do. But this language recites only functionality, i.e., no other structural components.

Similarly, Netlist’s citations to the specification cannot salvage its argument by identifying structure in the specification. *MTD Prods.*, 933 F.3d at 1344; *Williamson*, 792 F.3d at 1349 (“[t]he standard is whether the words of the claim [not the specification] are understood by [a POSITA] to have a sufficiently definite meaning as the name for structure.”).

In addition, Netlist’s reliance on claim language reciting how the “circuitry” is “coupled” and what the “circuitry” “includes,” *see, e.g.*, Op. Br., 21-22, does not impart sufficiently definite structure into the term “circuitry,” and therefore does not disqualify the claim from § 112(6) treatment. *See Williamson*, 792 F.3d at 1351. Here, like *MTD Products*, the claim language recites

purely functional language by describing what the “circuitry” is “configurable to” despite reciting how the “circuitry” is “coupled” to or “includes” other components. *MTD Prods.*, 933 F.3d at 1343. In doing so, “the claim format tends to favor [the] position that § 112, ¶ 6 applies.” *Id.*; see also *Williamson*, 792 F.3d at 1351.

Regarding corresponding structure, because § 112, ¶ 6 applies, claims 1, 6, and 11 are indefinite unless the ’417 patent’s specification discloses sufficient corresponding structure to perform the claimed functions. *Williamson*, 792 F.3d at 1351–52. It does not. Therefore, the claims are indefinite.

Here, the specification of the ’417 patent fails to describe any structure ***corresponding to the claimed functions*** of the means-plus-function “circuitry” limitations. Ex. AA, ¶¶ 55-57. Netlist does not indicate otherwise. For example, Netlist merely identifies numerous places where circuitry is ***generally described*** for transferring data bursts in the ’417 patent’s specification. See Op. Br., 23. However, nowhere in the disclosure of the ’417 patent cited by Netlist, or anywhere else, is there ***any disclosure of any structure that performs the specific “circuitry” functionality required by the claims***—enabling data transfers in response to the data buffer control signals. *Id.* Indeed, Netlist’s string citation falls far short of showing a clear link or association between a structure in the ’417 patent’s specification and the “circuitry” functionality at issue here. As such, the “circuitry” limitations are indefinite.

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**CERTIFICATE OF SERVICE**

I hereby certify that a true and correct copy of the foregoing document was filed electronically in compliance with Local Rule CV-5 on September 7, 2023. As of this date, all counsel of record have consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A).

/s/ Francis J. Albert